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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,302	03/06/2002	Yoshihiko Shimanuki	HITA.0176	8161

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EXAMINER
ZARNEKE, DAVID A

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,302	SHIMANUKI ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *81-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *81-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's argument with respect to the new limitation added into claim 81 regarding a plurality of external electrodes have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to the new limitation added into claim 81 regarding the plurality of external electrodes being between the edge of the chip and the edge of the device have been fully considered but they are not persuasive.

The examiner asserts that term "between" as used in the claims is the same as in Tsuji. Specifically, the electrode is formed within the boundary provided on one side by the chip and on the opposite side by the edge of the device. Applicant's argument with respect to the electrodes being formed underneath the chip is incorrect. The electrodes (34) to which the bond wires are attached are between the edge of the chip and the edge of the device (figure 13). Granted some electrodes (28) are underneath the chip, but the electrodes (34) to which the bond wires attach are between the edge of the chip and the edge of the device. These electrodes (34) are the ones that correspond to the electrodes in the claims, in that the claimed electrodes require bond wires to be attached and electrodes (34) of Tsuji are the ones that require bond wires.

Lastly, applicant argues that there is no motivation to combine Fujimoto with Tsuji.

The examiner points out that no such rejection was included in the office action; therefore, no further discussion of this is required.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 81-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al., US Patent 5,656,550, in view of Fjelstad, US Patent 6,294,830, or Fujimoto, US Patent 6,498,393.

Tsuji teaches a method of manufacturing a semiconductor device comprising the steps of:

providing a metal substrate (27) having a front surface, a rear surface, first grooves on the front surface partitioning the front surface in pads, second grooves on the rear surface, each of the second grooves being arranged directly opposite to one of the first grooves across the metal substrate (Figures 13A, 17A, 18A & 20C);

providing a semiconductor chip (41) having a front surface, a rear surface, electrodes formed on the front surface;

fixing the semiconductor chip on the front surface of the metal substrate;

forming an external electrode (34) between an edge of the semiconductor chip and an edge of the semiconductor device

electrically connecting the electrodes of the semiconductor chip with parts of the front surface of the metal substrate by conductive wires (43), respectively;

forming a resin body (23) which seals the semiconductor chip, the conductive wires, and the parts of the front surface of the metal substrate; and

after the resin body forming step, etching the rear surface of the metal substrate so as to expose bottoms of the second grooves and electrically isolating the pads of the front surface of the metal substrate (Figures 13B, 18B & 21B).

Tsuji fails to teach forming a plurality of rows of external electrodes in an area of the front surface of the metal substrate and isolating them from each other.

Fjelstad (figure 1D-2) and Fujimoto (figures) both teach forming a plurality of rows of external electrodes in an area of the front surface of the metal substrate and isolating them from each other.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the forming a plurality of rows of external electrodes in an area of the front surface of the metal substrate and isolating them from each other of Fjelstad and/or Fujimoto in the invention of Tsuji because, barring a showing of unexpected results, they both teach the conventionality of duplicating rows of external electrodes.

The mere duplication of parts has no patentable significance unless a new and unexpected result is produced. In re Harza, 124 USPQ 378 (CCPA 1960).

Though applicant argues that Fujimoto would not be combinable with Tsuji because it teaches conflicting external electrode arrangements, the examiner asserts that that would be a piecemeal analysis of the rejection and not considering the rejection as a whole. Which relies upon Fujimoto, and Fjelstad, to teach that a plurality of rows of external electrodes is known in the art.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections

are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Regarding claim 82, Tsuji teaches an etching step involving maintaining parts of the rear surface directly opposite to the parts of the front surface across the metal substrate un-etched so as to protrude therefrom at the bottoms of the second grooves (Figures 13B, 18B & 21B).

Regarding claim 83, while Tsuji teaches etching the rear surface of the metal substrate using a liquid (17, 34+), it would have been obvious to one of ordinary skill in the art to use immersion to apply the liquid because immersion is a conventionally known in the art technique to apply a liquid etchant.

The use of conventional materials to perform there known functions in a conventional process is obvious (*In re Raner* 134 USPQ 343 (CCPA 1962)).

With respect to claim 84, Tsuji teaches etching the bottom surface of the terminal outer terminal in order to separate the pole terminal portions and the frame terminal (12, 63+ & 15, 29+).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-F 10 AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David A. Zarneke
Primary Examiner
April 1, 2004